39. The semiconductor device according to claim 37 wherein said second impurity regions contain one of carbon, nitrogen and oxygen at a higher concentration than said first impurity regions.

40. The semiconductor device according to claim 37 wherein a distance between the channel forming region and the pair of first regions in said first thin film transistor is different from that of said second thin film transistor.

41. The semiconductor device according to claim 37 wherein said impurity is phosphorus.--

REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the present application.

The Examiner's non-final Office Action dated October 3, 2000 has been received and its contents carefully noted. Claims 1-36 were pending in the present application. By this amendment, claim 19 has been amended, claims 26-33 have been canceled, and claims 37-41 have been added. Accordingly, claims 1-25 and 34-41 are currently pending, of which 1, 6, 11, 16, 19, and 37 are independent.

Referring now to the Office Action, the Examiner indicated that an earlier submitted IDS did not contain copies of the documents cited therein. Accordingly, Applicants are in the process of obtaining copies of the foreign patents and non-patent publications and will submit a Supplemental Information Disclosure Statement as soon as possible.

With respect to the drawings, Fig. 4 is objected as not properly labeled as "Prior Art", and Fig. 8B is not labeled with "ya'" as described in page 17, line 20 of the specification and "FTT" mislabeled. Applicants are submitting herewith a corrected Fig. 4 with "Prior Art" label added in red ink, as well as Fig. 8B with --ya'-- and --TFT-- corrected in red ink, and a letter to the Official Draftsperson requesting review and consideration of the corrections.

With respect to the drawing objection under 37 CFR 1.83(a), Applicants are preparing a new drawing showing the feature of the invention specified in claims 5, 10, 15, 23, and 30 and disclosed in page 4 of the specification. Accordingly, it is respectfully requested that the objection be held in abeyance until all the pending claims are allowed.

Claim 19 stands rejected under 35 U.S.C. § 112, second paragraph for lacking proper antecedent basis for the feature "second thin film transistor". Applicants have amended claim 19, as shown above to delete the word "second" as it was not intended to be in the claim. Accordingly, it is respectfully requested that the § 112 rejection of claim 19 be reconsidered and withdrawn.

Claims 1-36 stand rejected under the judicially created double patenting doctrine of obviousness-type as allegedly unpatentable over claims 1-18 of U.S. Patent No. 5,962,872. This rejection is respectfully traversed.

Applicants respectfully submit that the presently claimed invention distinguishes over claims 1-18 of the '872 patent by reciting at least a feature including an overlap between the gate electrode and the second impurity regions, as claimed in independent claims 1, 6, 11, 16, and 19.

In a TFT of a driver circuit, typically in an NTFT, it is advantageous to make the gate electrode overlap with the second impurity regions in order to avoid a problem caused by hot carriers. Accordingly, the double patenting rejection of claims 1-36 is insupportable and is respectfully requested to be reconsidered and withdrawn.

With respect to claims 5, 10, 15, 23, and 30, the Office applied Hohjo (U.S. Patent No. 5,028,551) in presumably a 35 U.S.C. § 103 rejection. With respect to claim 16, the Office applied Shimada et al. (EP 488801A1) in presumably a 35 U.S.C. § 103 rejection. These rejection are respectfully traversed at least for the reason set forth above with respect to the double patenting rejection over the '872 patent.

Applicants respectfully submit that none of the cited prior art references teach, suggest, or imply a gate electrode overlapped with the second impurity regions as recited in Applicants' claimed invention. Further, none of the cited prior art references teach or motivate one of ordinary skills in the art to combine their various and different teachings to make Applicants'

claimed invention. Accordingly, the rejections based on the cited prior art references are insupportable and are requested to be reconsidered and withdrawn.

Applicants note that the burden of establishing a prima facie case of obviousness under §103 lies with the Patent Office. In re Fine, 5 USPQ2d 1596 (Fed. Cir. 1988). To establish a prima facie case of obviousness, there must be (1) some suggestion or motivation (either in the references themselves or in the knowledge generally available to one of ordinary skill in the art) to modify the reference or to combine reference teachings to achieve the claimed invention and (2) the prior art must teach or suggest all the claim limitations. MPEP § 2143. Also, simply because the references could be does not mean that they should be. MPEP § 2143.01, citing In re Mills, 16 USPQ2d 1430 (Fed. Cir. 1990).

With respect to the rejection of claims 6, 11, 17, 18, 31, and 32, Applicants respectfully submit that routine experimentation is not sufficient for providing the required motivation for a obviousness rejection. Nothing in the prior art references cited in the Office Action would suggest the necessity or desirability of a distance between the channel forming region and the pair of first regions in the thin film transistor being within the range of 0.4 to 2 μm. Obviousness does not require absolute predictability but a reasonable expectation of success is necessary. In re Clinton, 188 USPQ 365, 367 (CCPA 1976) *(emphasis added)*. Both the suggestion of the invention and the expectation of success must be found in the prior art, not in Applicants' disclosure. Selective hindsight is not appropriate to design experiments in order to reach the claimed invention. In re Dow Chemical, 5 USPQ2d 1529, 1531-32 (Fed. Cir. 1988).

In view of the above Applicants respectfully submit that a prima facie showing of obviousness has not been made in this case. As such, Applicants respectfully requests that the rejection of claims 2-32, and 34-36 be reconsidered and withdrawn.

Claims 26-33 have been canceled in as much as these claims do not recite an overlap between the gate electrode and the second impurity regions. Accordingly, all the rejections on these claims are now moot.

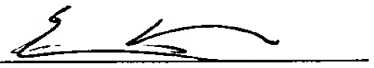
New claims 37-41 have been added to cover the scope of protection in which Applicants are entitled. No new matter has been added. Support for these claims can be found at least in, e.g., Figs. 8A and 8B and corresponding descriptions in the specification.

CONCLUSION

Having responded to all rejections set forth in the outstanding non-final Office Action, it is submitted that claims 1-25, 34-36, and new claims 37-41 are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,

NIXON PEABODY, LLP

By 

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VERSION OF AMENDED CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

19. (Amended) A semiconductor device including at least one thin film transistor, said thin film transistor comprising:

a gate electrode;

a gate insulating film adjacent to the gate electrode; and

a semiconductor film adjacent to said gate insulating film wherein said semiconductor film includes a channel forming region, a pair of first regions containing an impurity for giving one conductivity type thereto with said channel forming region therebetween, and a pair of second regions in which a concentration of said impurity is smaller than that in said first regions wherein said second regions are interposed between said channel forming region and said pair of first regions,

wherein the pair of second regions are overlapped with the gate electrode of said [second] thin film transistor.